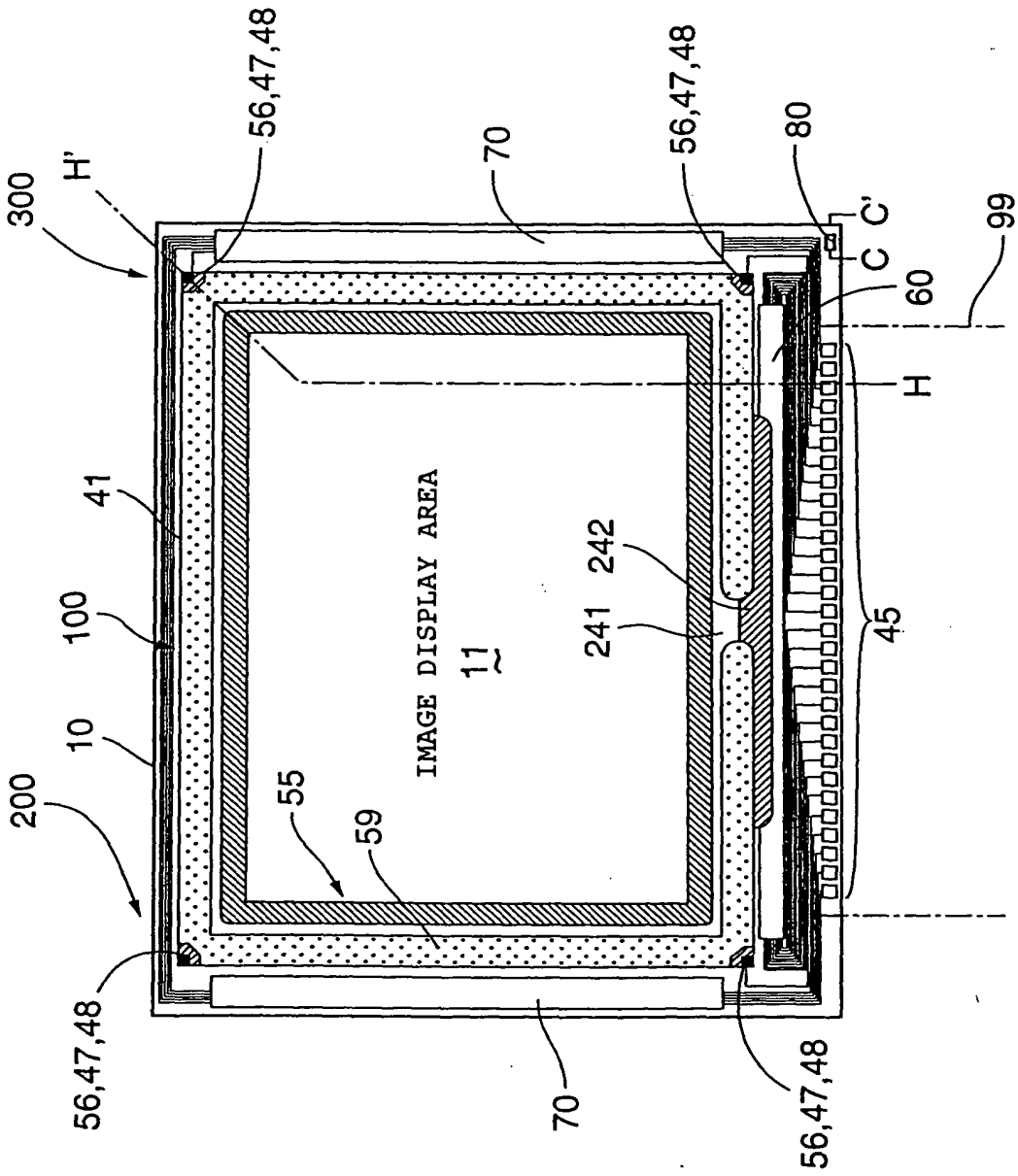

300
H'
56,47,48
70
56,47,48
80
C
C'
99
60
H
41
100
10
200
IMAGE DISPLAY AREA
11
241
242
45
55
59
56,47,48
70
56,47,48

FIG. 1

FIG. 2

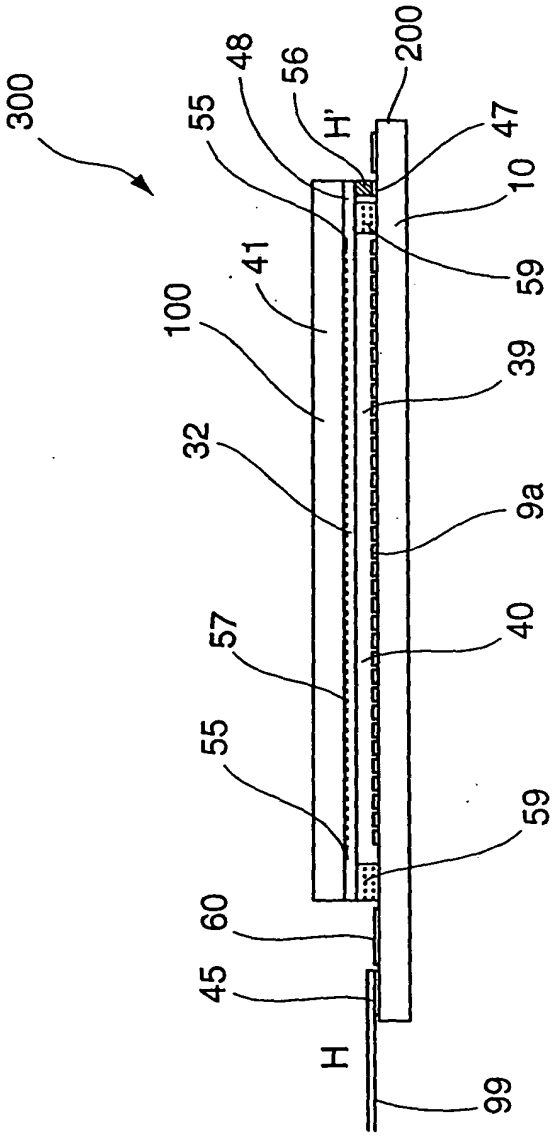


FIG. 3

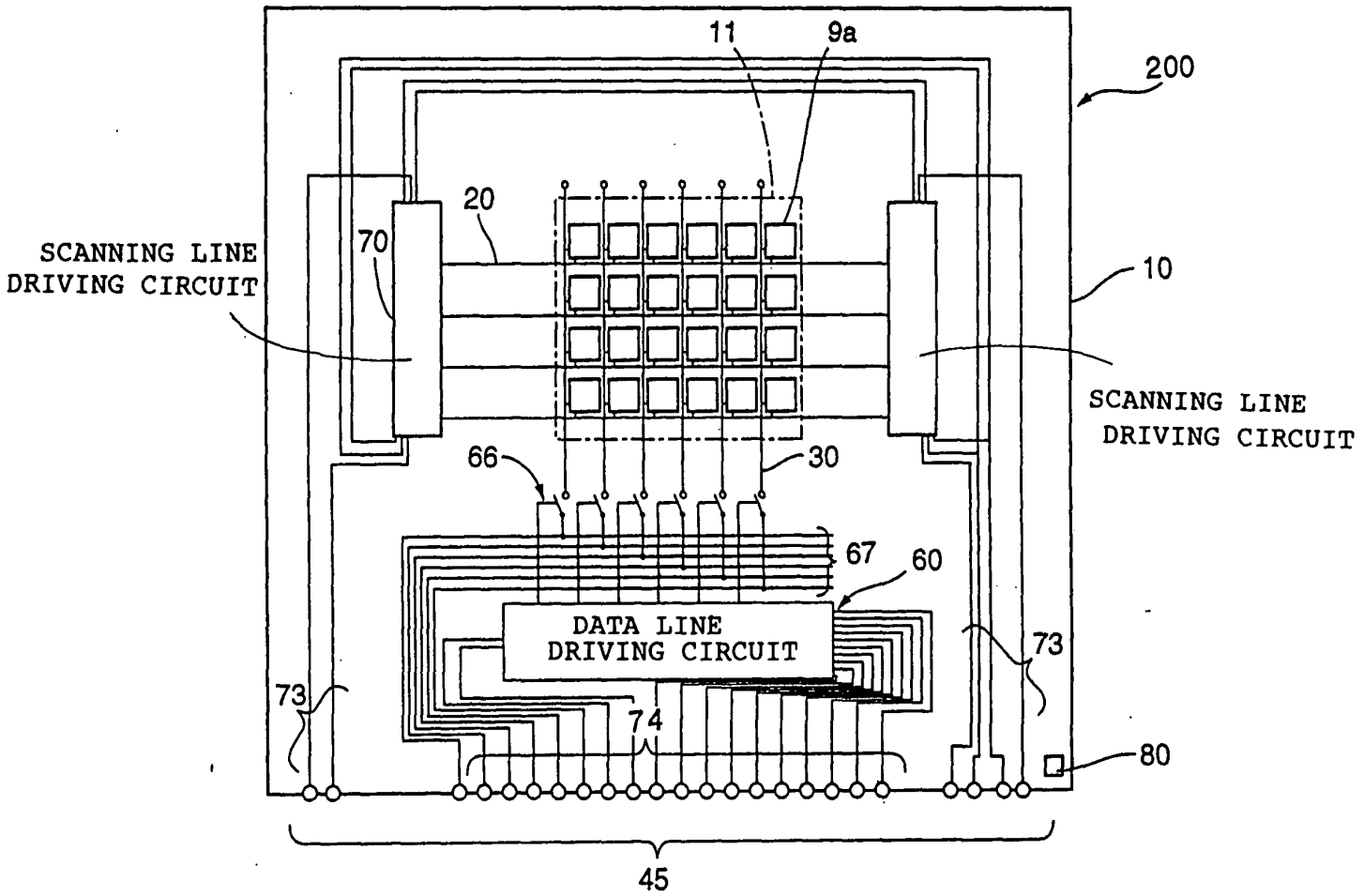

11
9a
200
20
70
SCANNING LINE
DRIVING CIRCUIT
10
SCANNING LINE
DRIVING CIRCUIT
66
30
67
60
DATA LINE
DRIVING CIRCUIT
73
73
74
80
45

FIG. 4

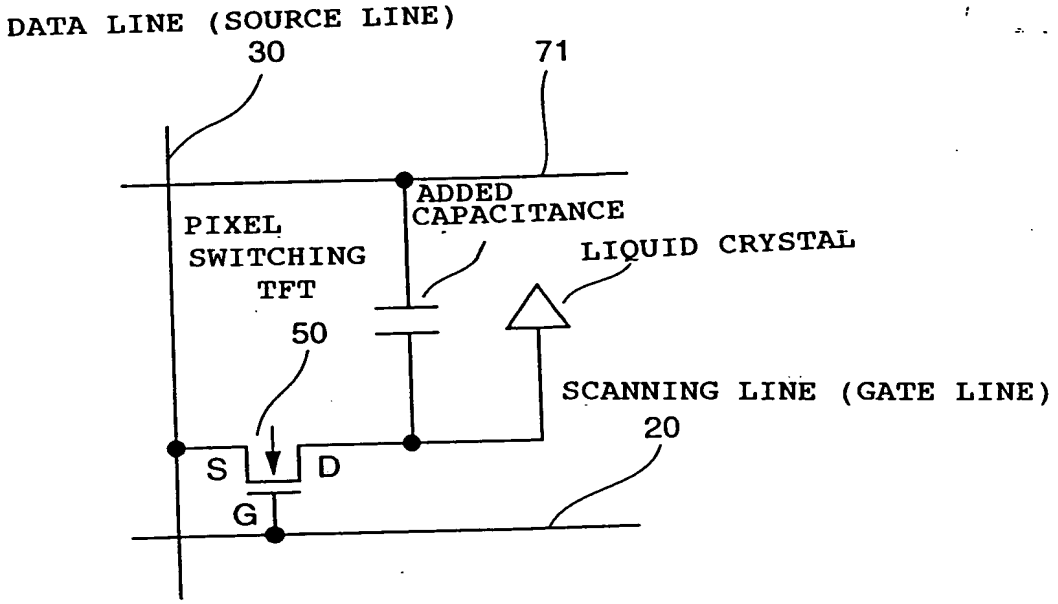

DATA LINE (SOURCE LINE)
30
71
ADDED
CAPACITANCE
PIXEL
SWITCHING
TFT
LIQUID CRYSTAL
50
SCANNING LINE (GATE LINE)
20
S
D
G

FIG. 5

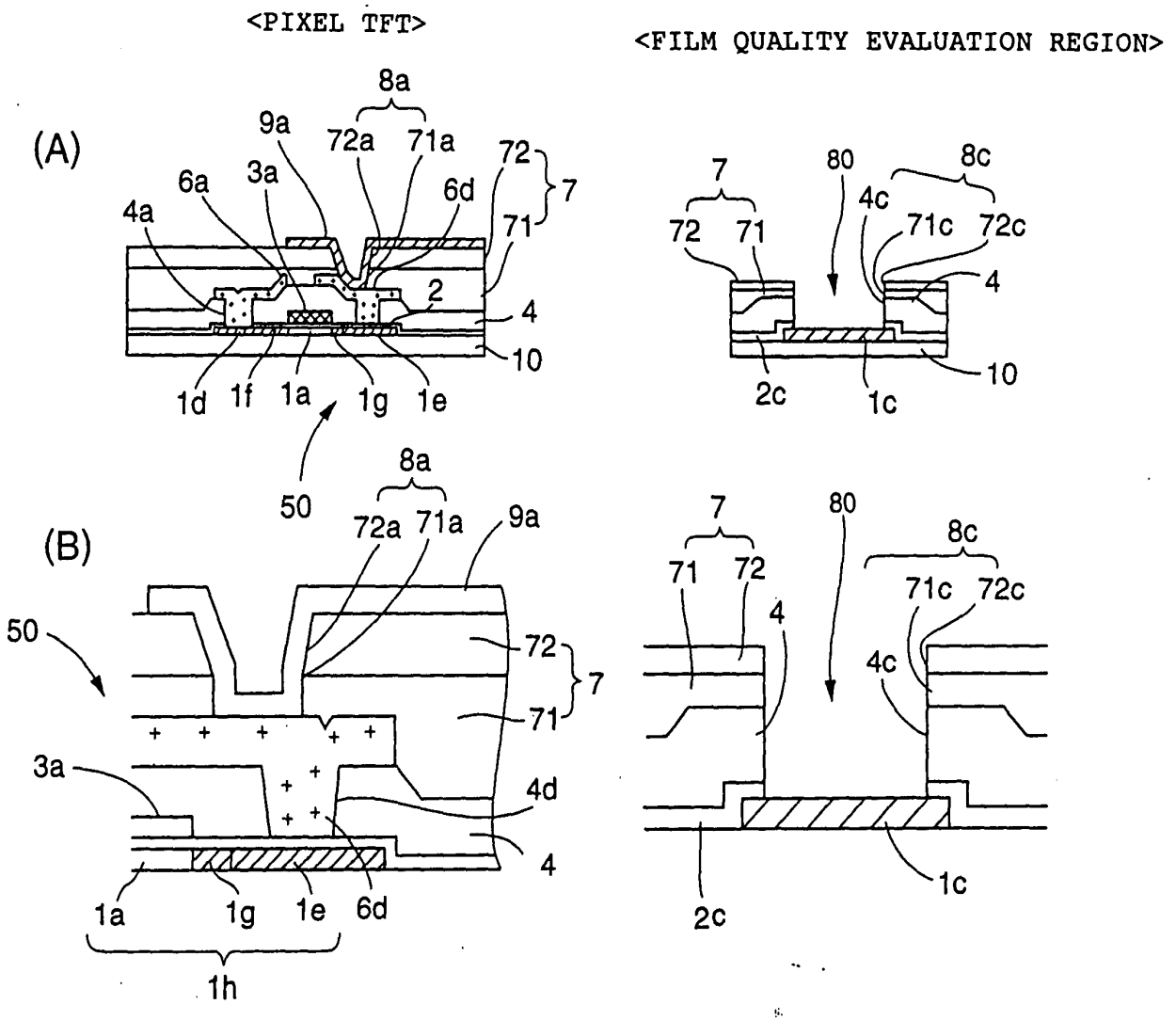

<PIXEL TFT>
<FILM QUALITY EVALUATION REGION>
(A)
(B)
8a
9a
72a
71a
72
7
6a
3a
6d
4a
71
2
4
10
1d
1f
1a
1g
1e
50
80
8c
4c
71c
72c
2c
1c
3a
4d
1h

FIG. 6

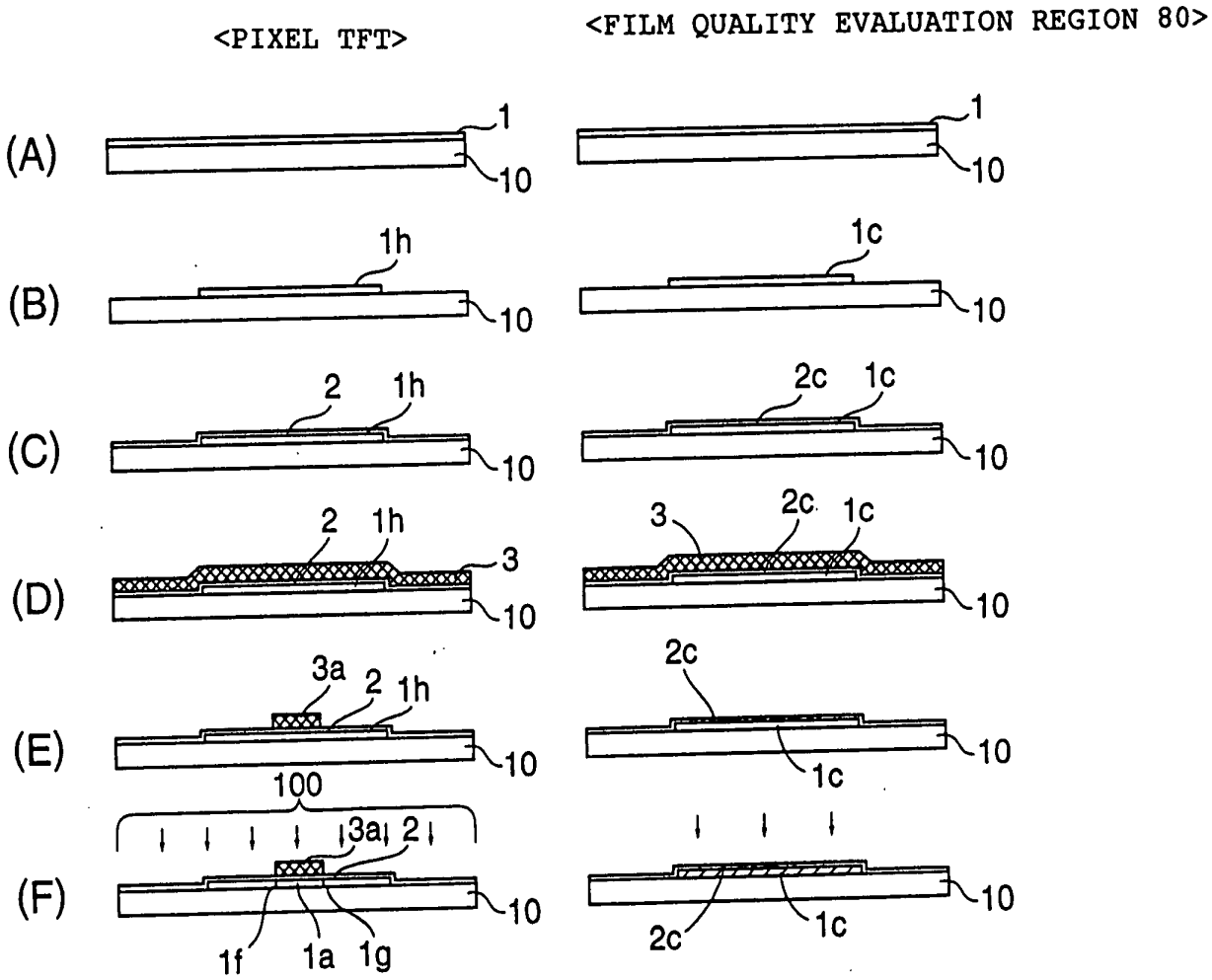

<PIXEL TFT>
<FILM QUALITY EVALUATION REGION 80>
(A)
(B)
(C)
(D)
(E)
(F)
1
10
1h
1c
2
2c
3
3a
100
1f
1a
1g

FIG. 7

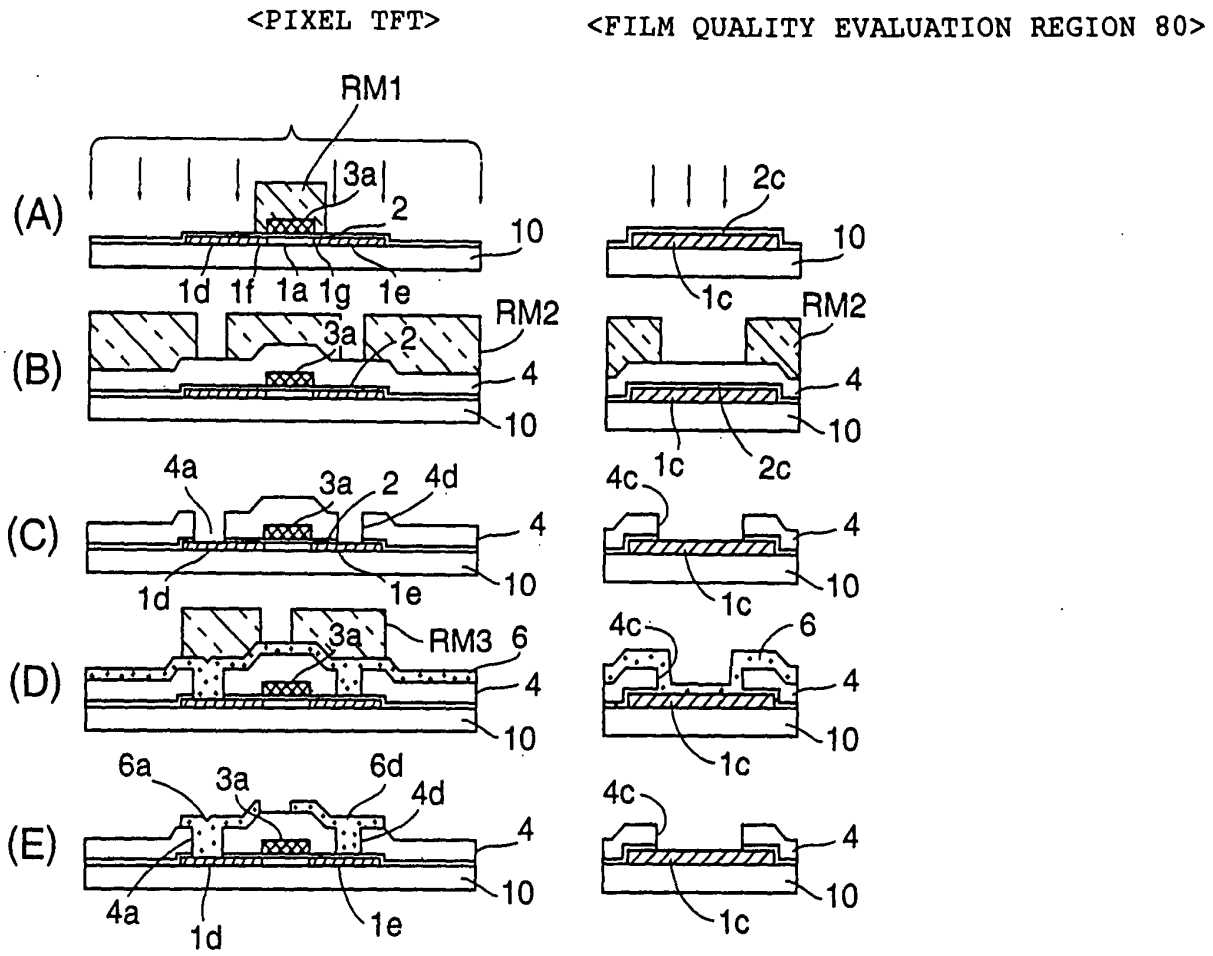

<PIXEL TFT>
<FILM QUALITY EVALUATION REGION 80>
(A)
(B)
(C)
(D)
(E)
RM1
RM2
RM3
3a
2
2c
10
1d
1f
1a
1g
1e
1c
4
4a
4d
4c
6
6a
6d

FIG. 8

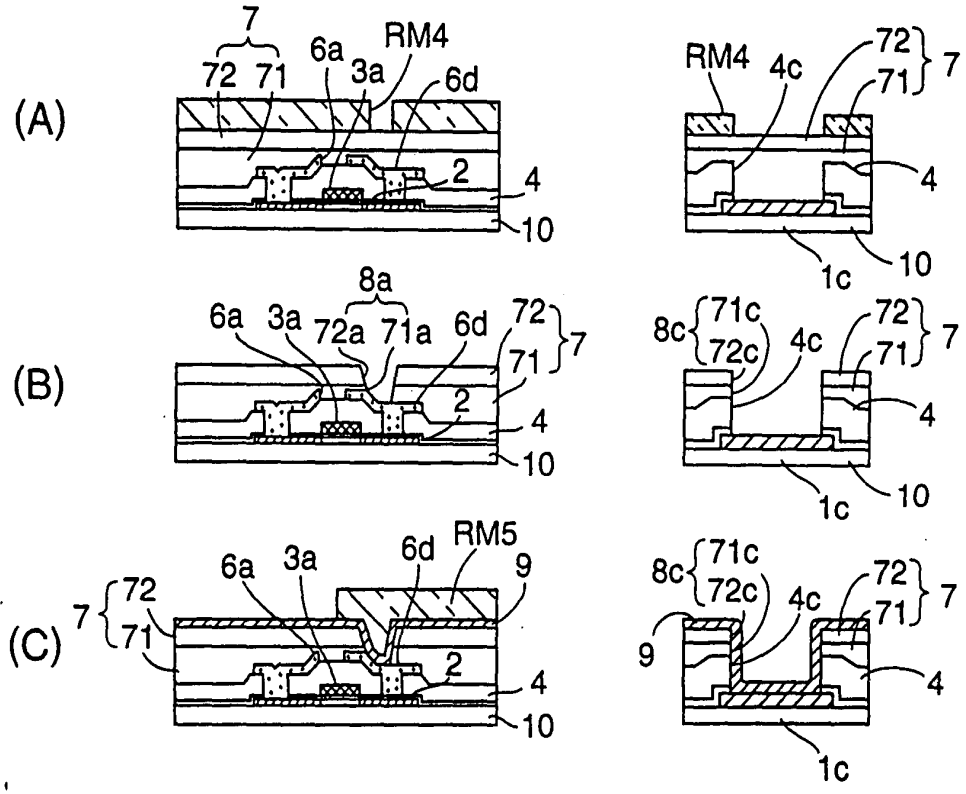

<PIXEL TFT>
<FILM QUALITY EVALUATION REGION 80>
(A)
(B)
(C)
7
72
71
6a
3a
RM4
6d
2
4
10
1c
8a
72a
71a
RM5
9
8c
71c
72c
4c

FIG. 9

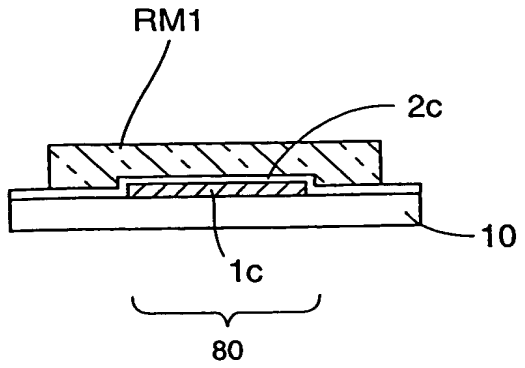
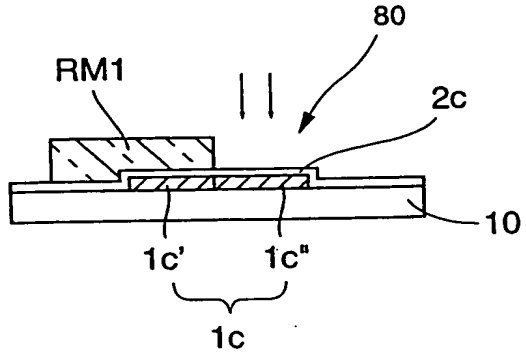


FIG. 10 (A)



(B)

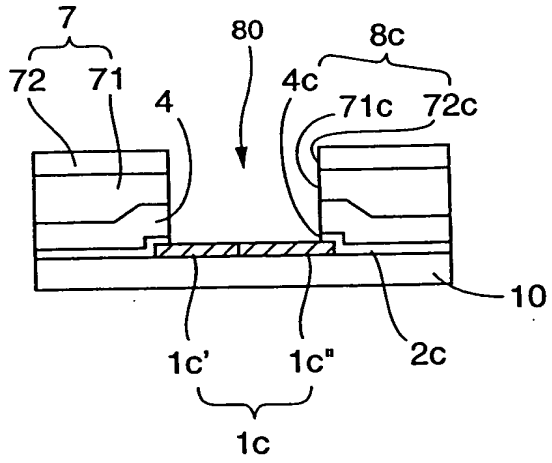


FIG. 11

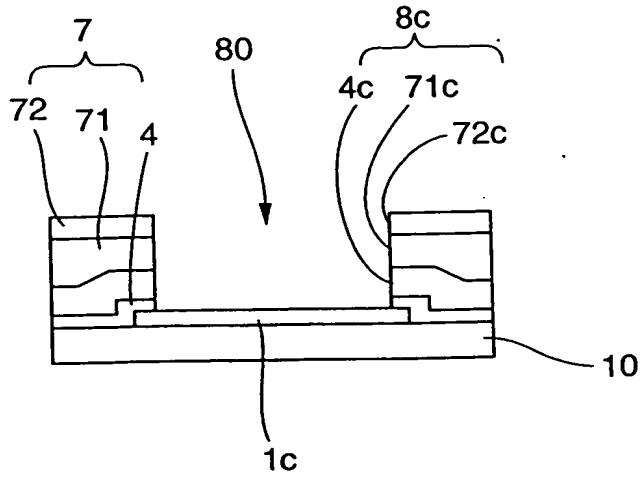

7
8c
80
72
71
4
4c
71c
72c
10
1c

FIG. 12

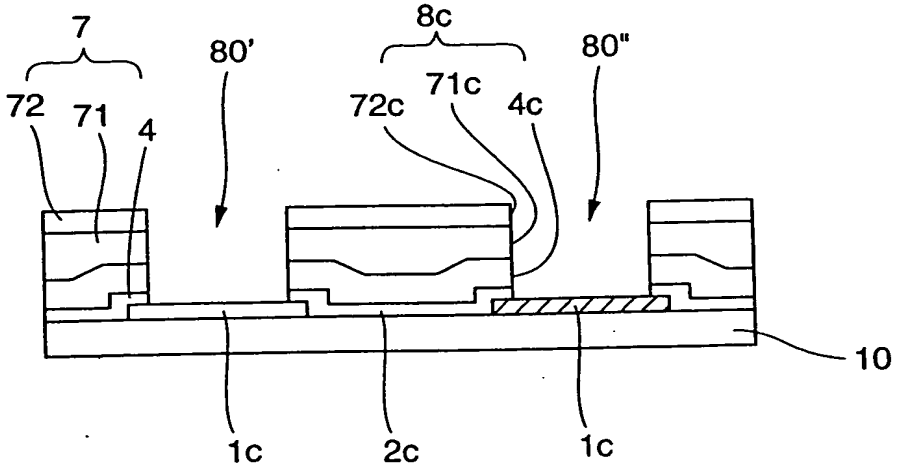

7
80'
8c
80"
72
71
4
72c
71c
4c
10
1c
2c
1c

FIG. 13

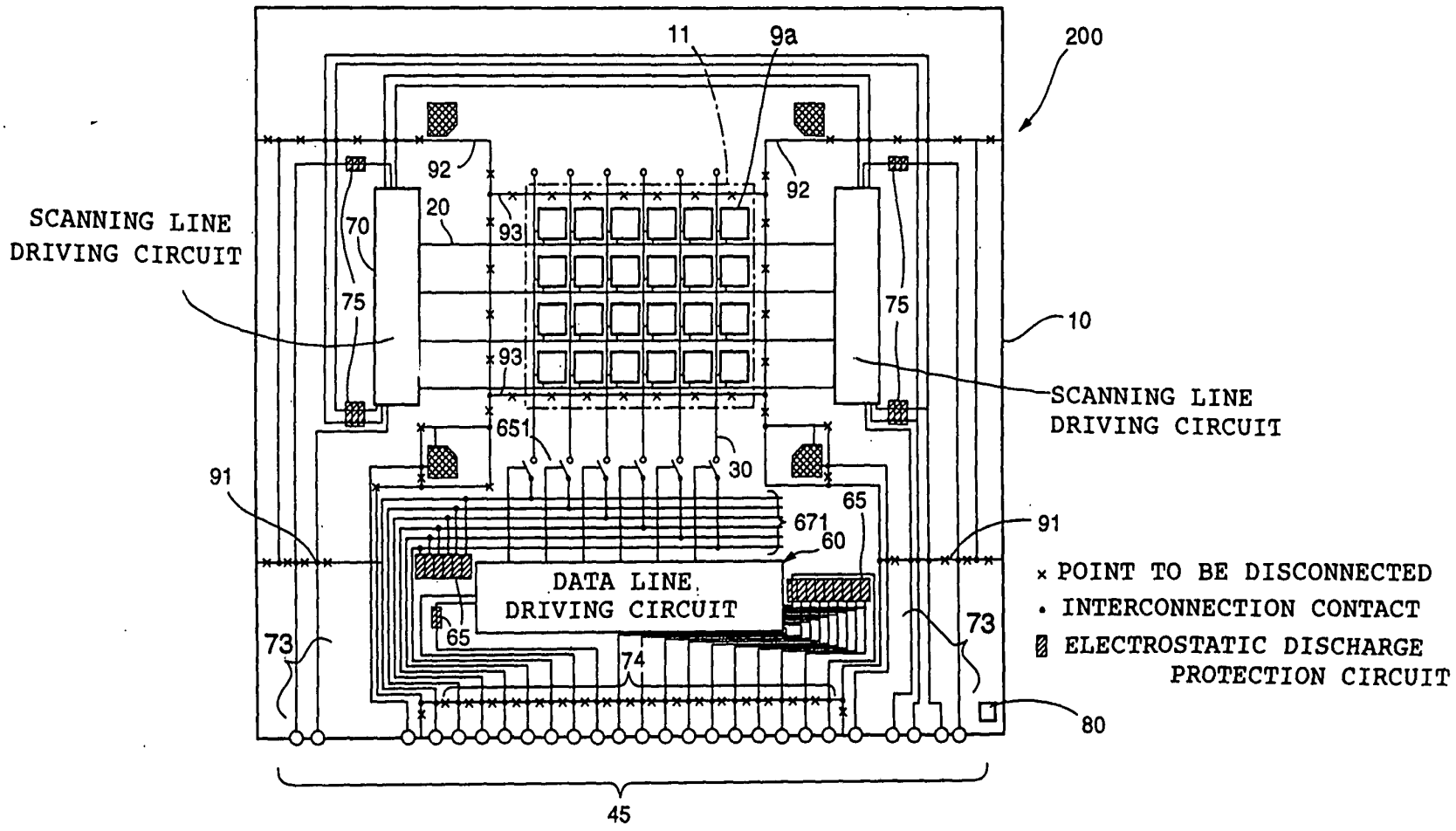
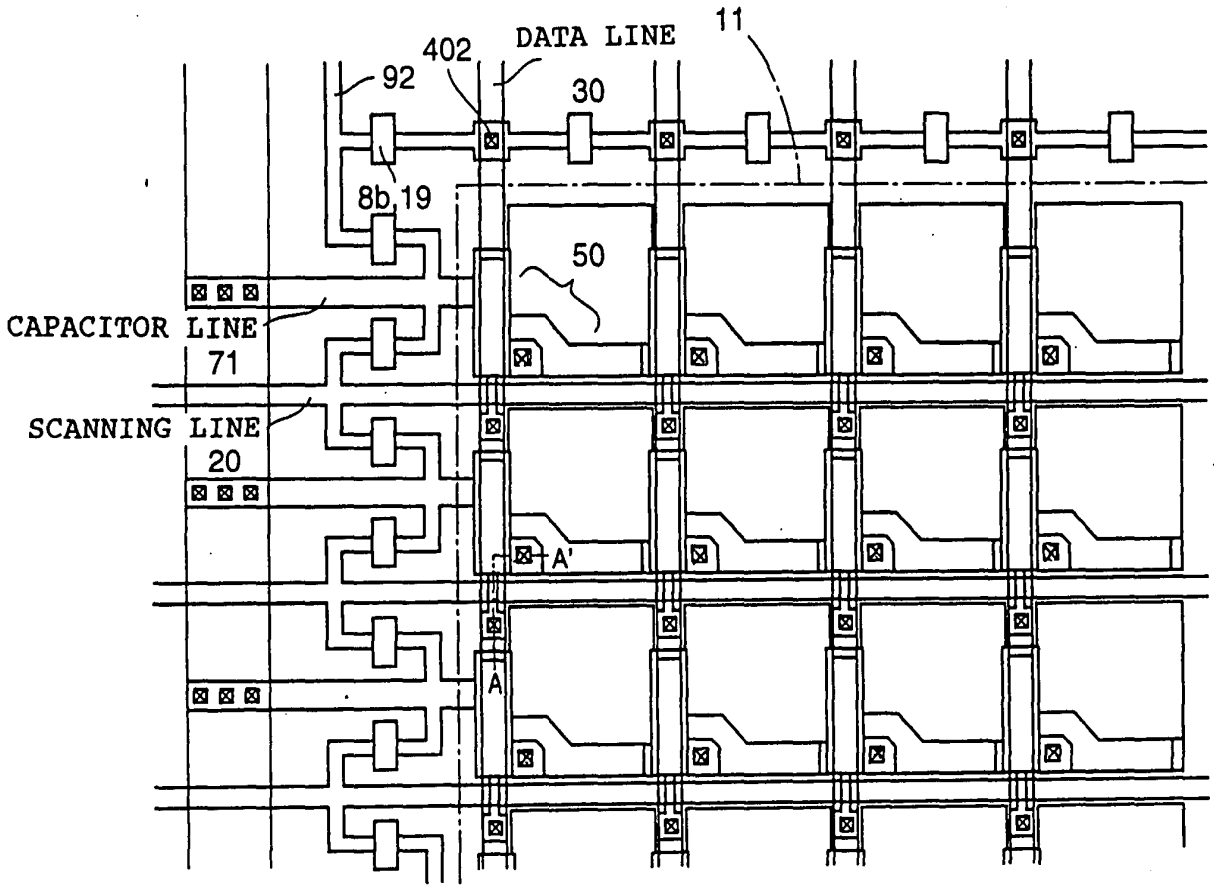

11
9a
200
92
92
SCANNING LINE
DRIVING CIRCUIT
20
70
93
75
75
10
93
SCANNING LINE
DRIVING CIRCUIT
651
30
91
65
671
91
60
DATA LINE
DRIVING CIRCUIT
× POINT TO BE DISCONNECTED
• INTERCONNECTION CONTACT
ELECTROSTATIC DISCHARGE
PROTECTION CIRCUIT
73
65
74
73
80
45

FIG. 14



<PLAN VIEW OF A CORNER OF IMAGE DISPLAY AREA>

FIG. 15

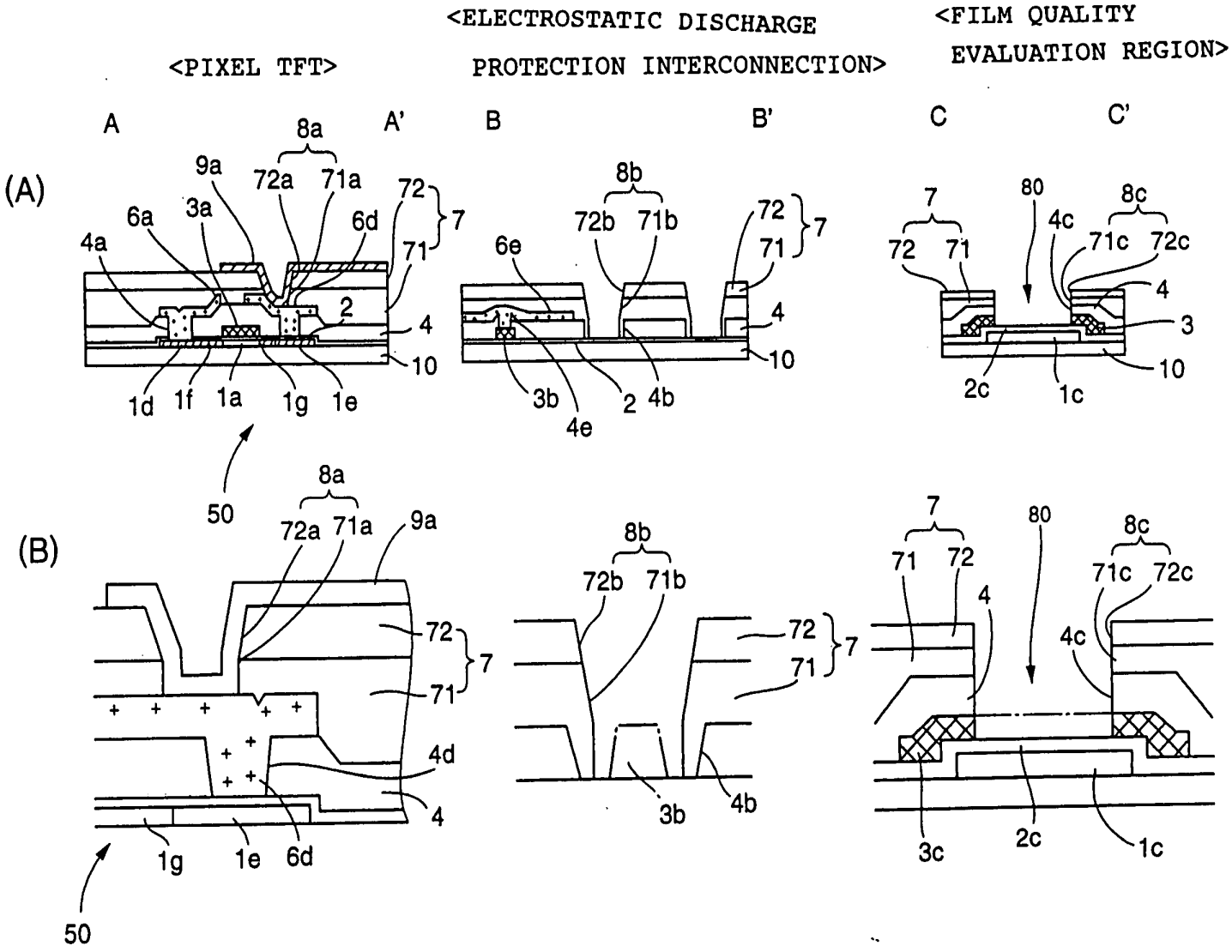

<PIXEL TFT>
<ELECTROSTATIC DISCHARGE PROTECTION INTERCONNECTION>
<FILM QUALITY EVALUATION REGION>
A
A'
B
B'
C
C'
(A)
(B)
8a
9a
72a
71a
72
7
71
6a
3a
6d
4a
2
4
10
1d
1f
1a
1g
1e
50
8b
72b
71b
6e
3b
4e
4b
80
8c
4c
71c
72c
3
2c
1c
3c
4d

FIG. 16

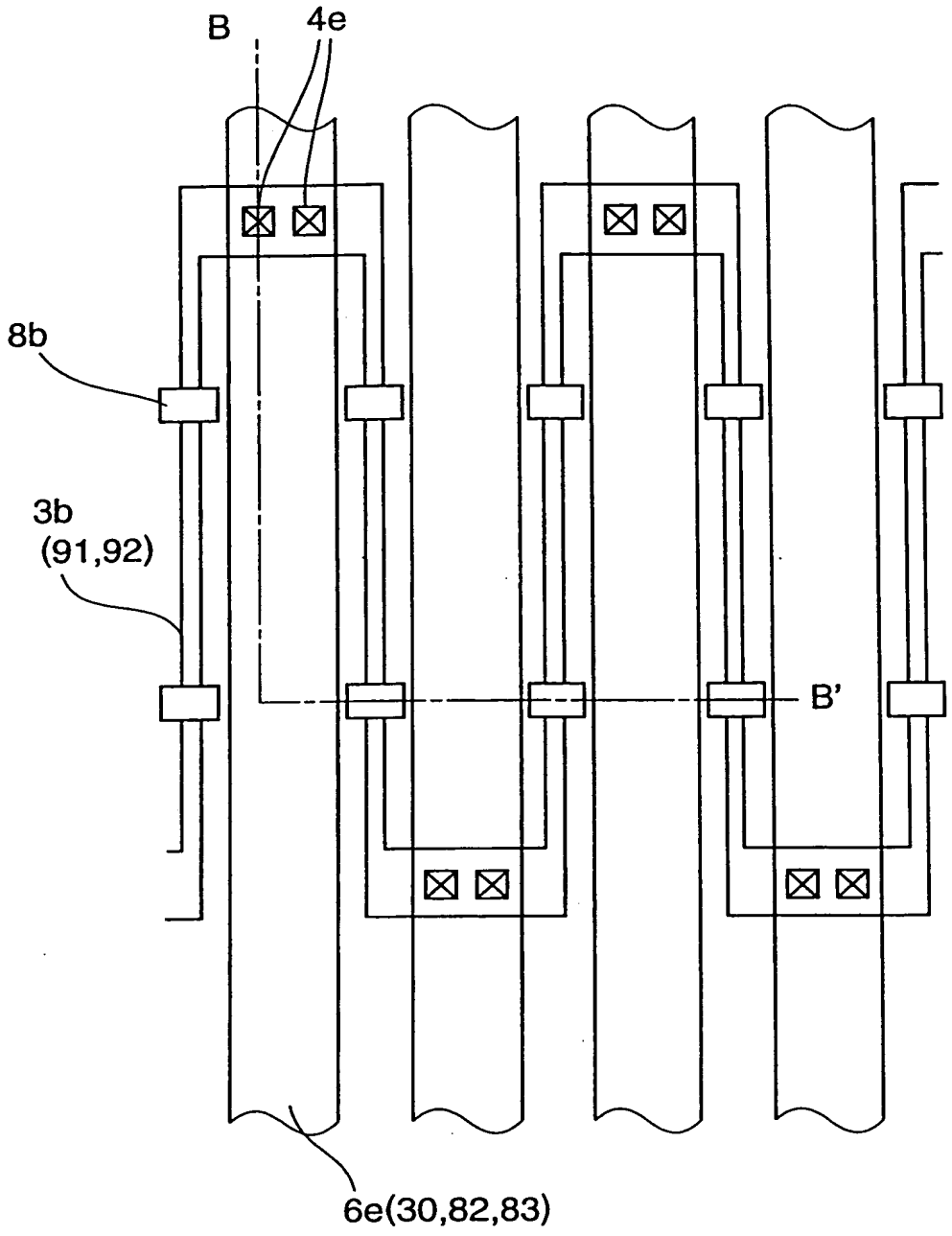


FIG. 17

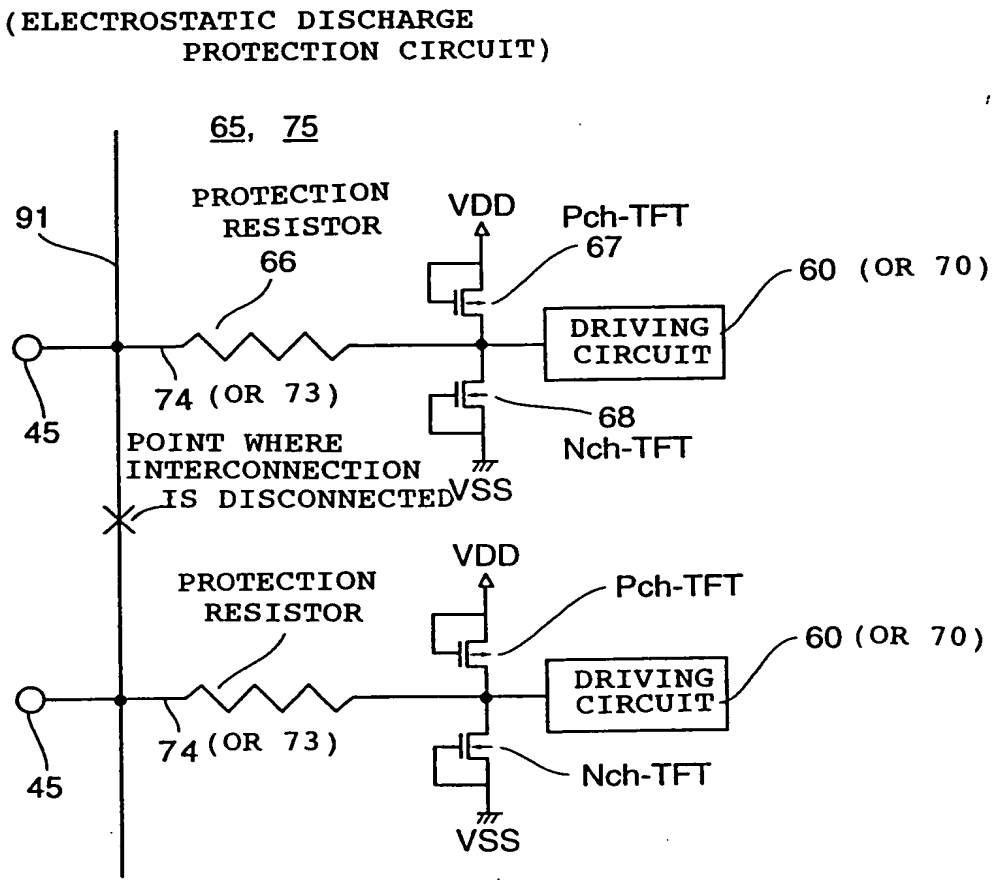

(ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT)
65, 75
91
PROTECTION RESISTOR
66
VDD
Pch-TFT
67
60 (OR 70)
DRIVING CIRCUIT
74 (OR 73)
45
68
Nch-TFT
POINT WHERE INTERCONNECTION IS DISCONNECTED
VSS
VDD
PROTECTION RESISTOR
Pch-TFT
60 (OR 70)
DRIVING CIRCUIT
74 (OR 73)
45
Nch-TFT
VSS

FIG. 18

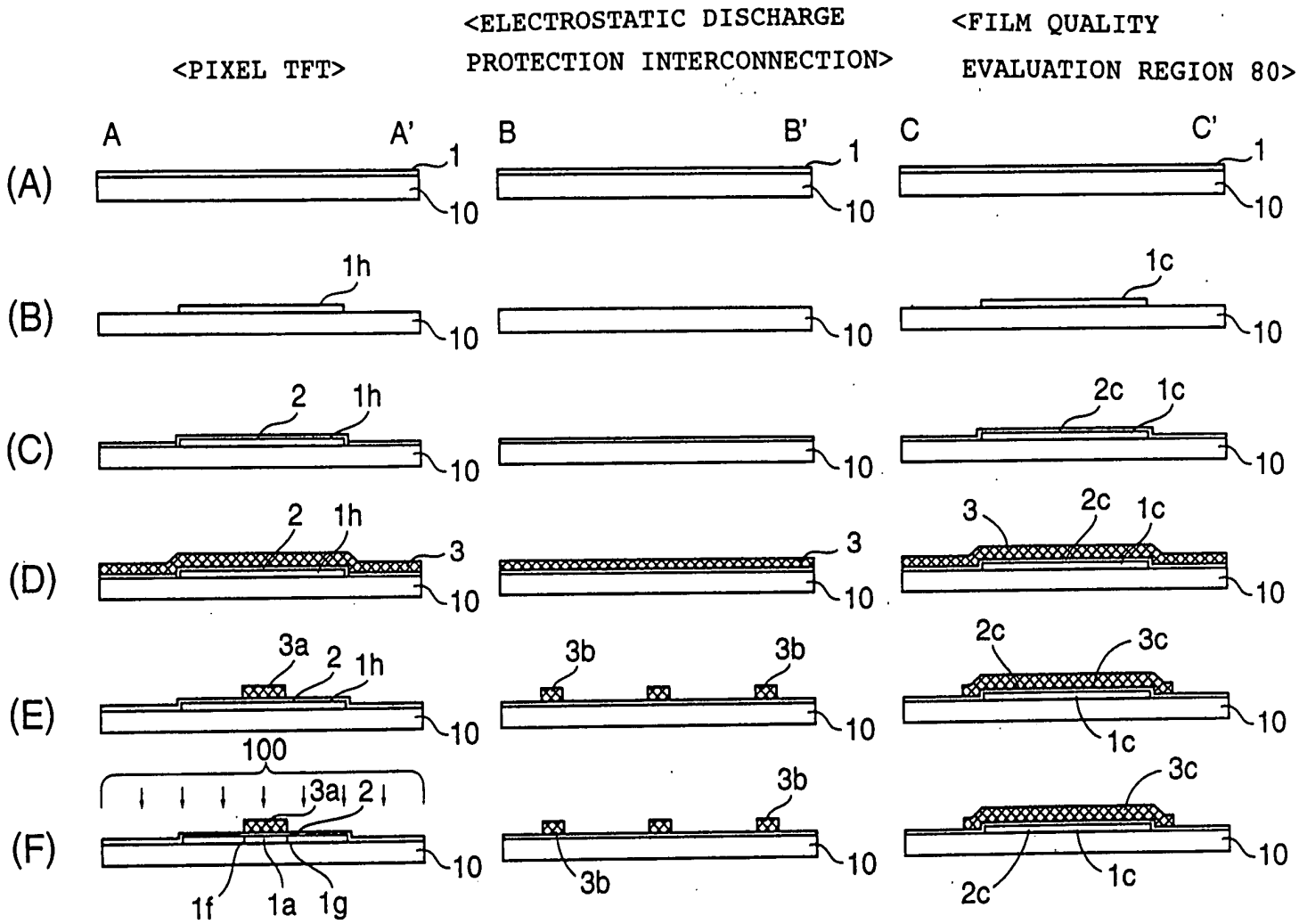

<PIXEL TFT>
<ELECTROSTATIC DISCHARGE PROTECTION INTERCONNECTION>
<FILM QUALITY EVALUATION REGION 80>
A
A'
B
B'
C
C'
(A)
(B)
(C)
(D)
(E)
(F)
1
10
1h
1c
2
2c
3
3a
3b
3c
100
1f
1a
1g

FIG. 19

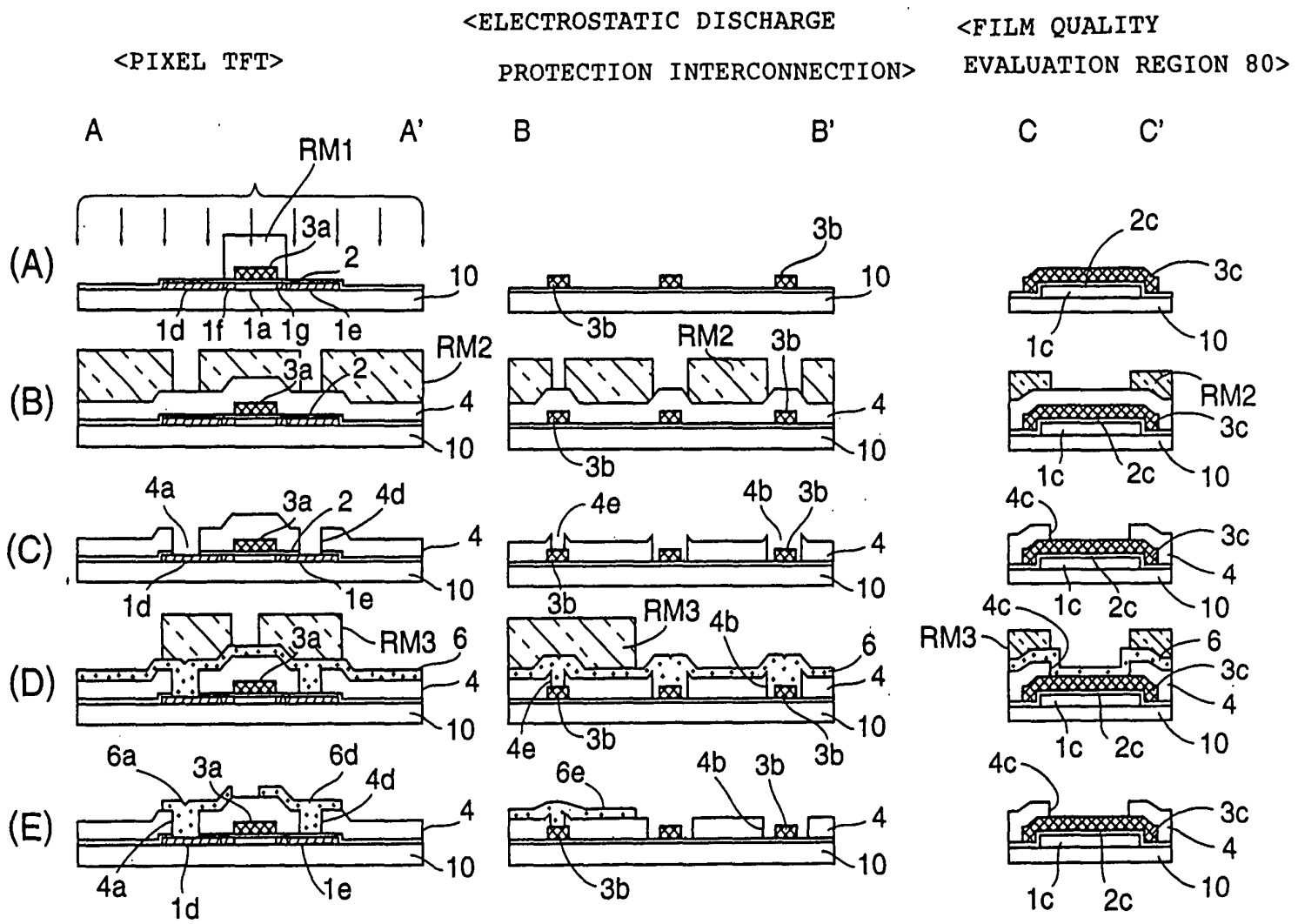

<PIXEL TFT>
<ELECTROSTATIC DISCHARGE PROTECTION INTERCONNECTION>
<FILM QUALITY EVALUATION REGION 80>
A
A'
B
B'
C
C'
(A)
(B)
(C)
(D)
(E)
RM1
RM2
RM3
3a
3b
2
2c
3c
10
1d
1f
1a
1g
1e
1c
4
4a
4b
4c
4d
4e
6
6a
6d
6e

FIG. 20

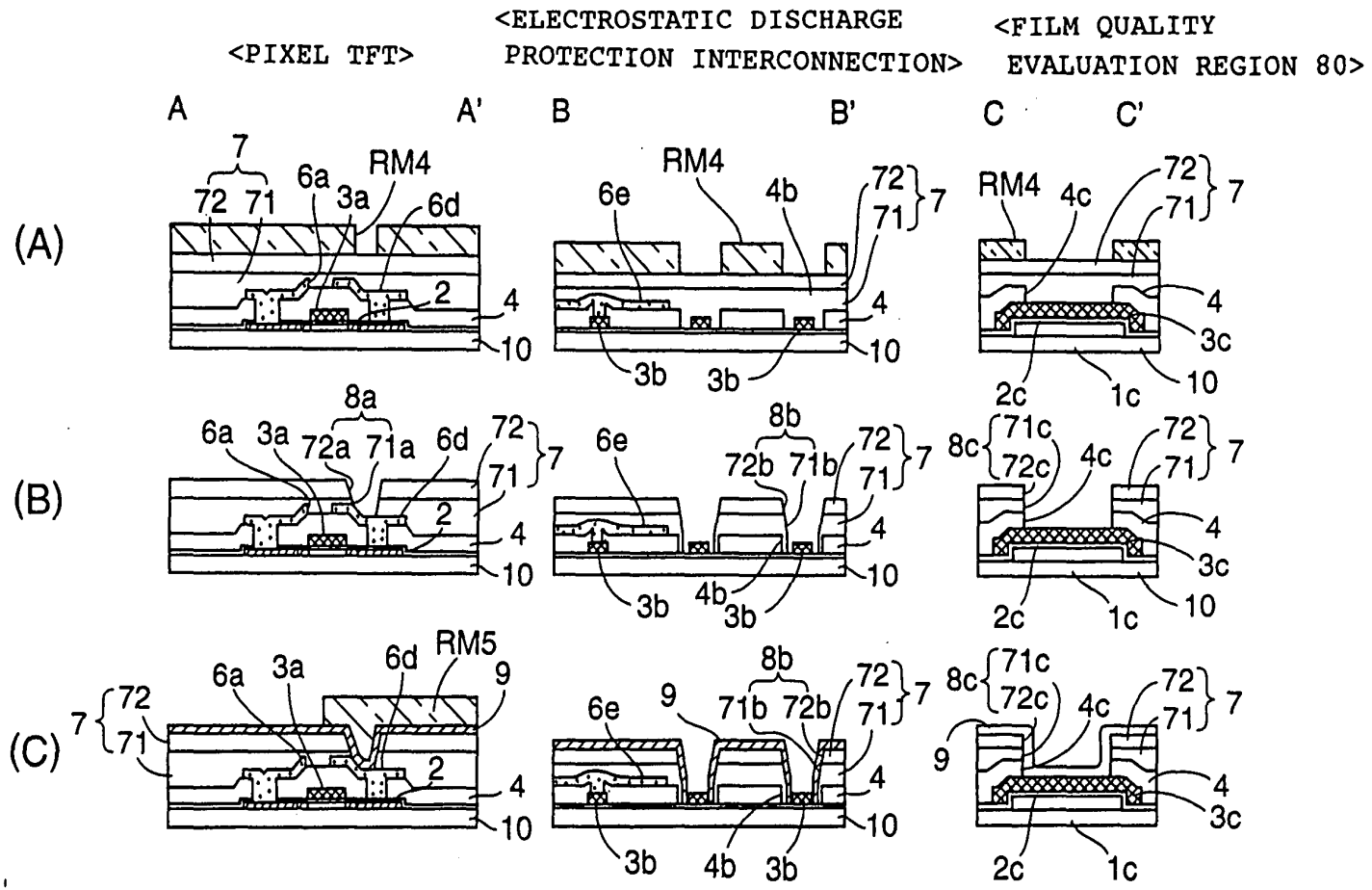

<PIXEL TFT>
<ELECTROSTATIC DISCHARGE PROTECTION INTERCONNECTION>
<FILM QUALITY EVALUATION REGION 80>
A
A'
B
B'
C
C'
(A)
(B)
(C)
7
72
71
6a
3a
RM4
6d
2
4
10
6e
4b
3b
4c
3c
2c
1c
8a
72a
71a
8b
72b
71b
8c
71c
72c
RM5
9

FIG. 21